Fig. 1

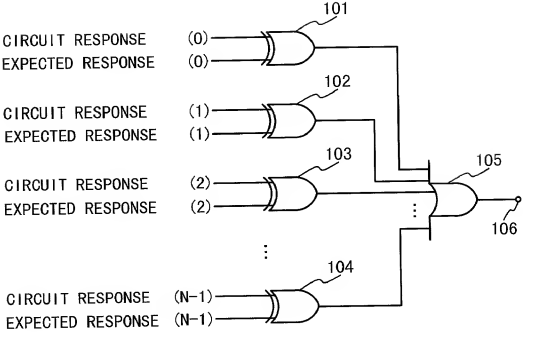
101
CIRCUIT RESPONSE
EXPECTED RESPONSE
(0)
(0)
102
CIRCUIT RESPONSE
EXPECTED RESPONSE
(1)
(1)
103
CIRCUIT RESPONSE
EXPECTED RESPONSE
(2)
(2)
105
106
104
CIRCUIT RESPONSE
EXPECTED RESPONSE
(N-1)
(N-1)

Fig. 2

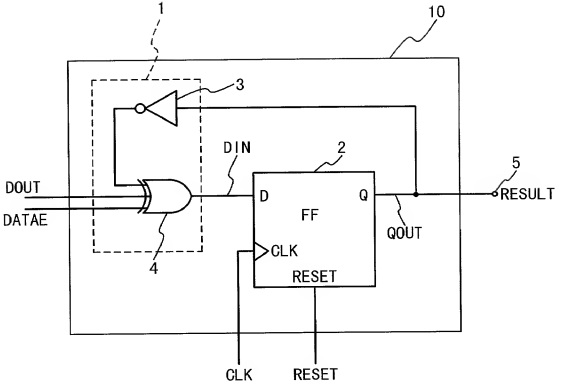

Fig. 3

DOUT	DATAE	QOUT	DIN
0	0	0	1
1	0	0	0
0	1	0	0
1	1	0	1
0	0	1	0
1	0	1	1
0	1	1	1
1	1	1	0

Fig. 4

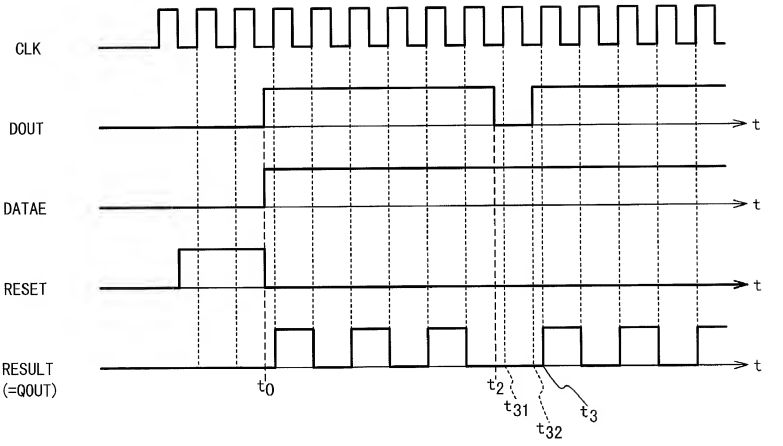

Fig. 5

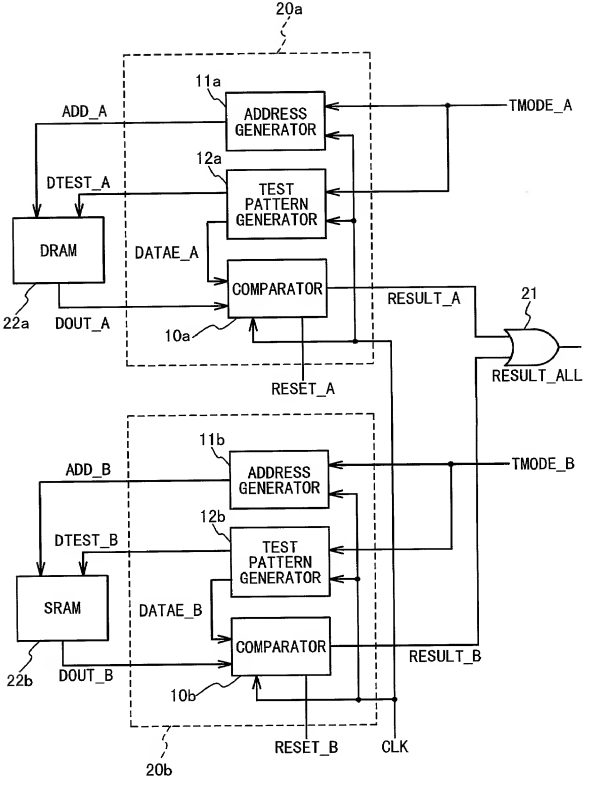
20a
11a
ADDRESS GENERATOR
ADD_A
TMODE_A
12a
TEST PATTERN GENERATOR
DTEST_A
DRAM
DATAE_A
COMPARATOR
RESULT_A
21
22a
DOUT_A
10a
RESULT_ALL
RESET_A
11b
ADDRESS GENERATOR
ADD_B
TMODE_B
12b
TEST PATTERN GENERATOR
DTEST_B
SRAM
DATAE_B
COMPARATOR
RESULT_B
22b
DOUT_B
10b
RESET_B
CLK
20b

Fig. 6

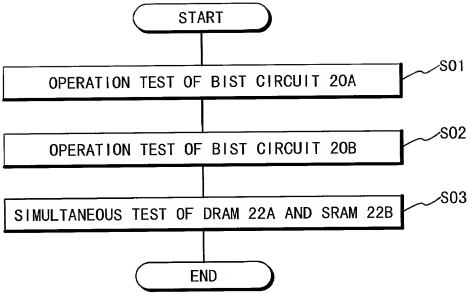
START
OPERATION TEST OF BIST CIRCUIT 20A
S01
OPERATION TEST OF BIST CIRCUIT 20B
S02
SIMULTANEOUS TEST OF DRAM 22A AND SRAM 22B
S03
END

Fig. 7

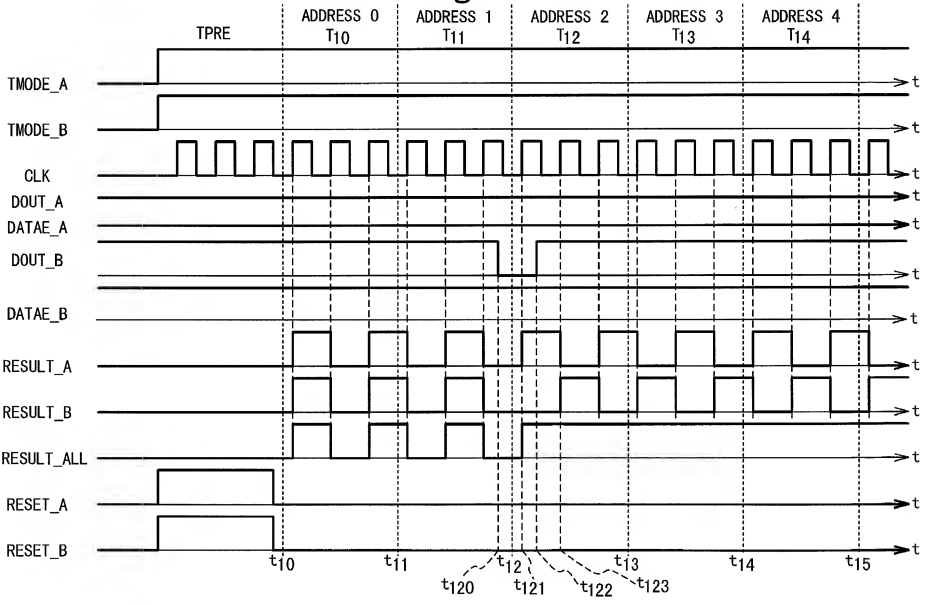

Fig. 8

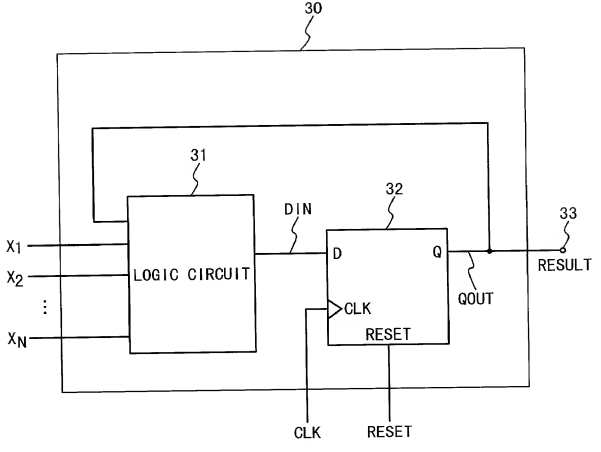
30
31
32
33
DIN
X1
X2
XN
LOGIC CIRCUIT
D
Q
CLK
RESET
QOUT
RESULT
CLK
RESET

Fig. 9